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PAPER

Toward active-matrix lab-on-a-chip: programmable electrofluidic control enabled by arrayed oxide thin film transistors†

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Agile micro- and nano-fluidic control is critical to numerous life science and chemical science synthesis as well as kinetic and thermodynamic studies. To this end, we have demonstrated the use of thin film transistor arrays as an active matrix addressing method to control an electrofluidic array. Because the active matrix method minimizes the number of control lines necessary ($m + n$ lines for the $m \times n$ element array), the active matrix addressing method integrated with an electrofluidic platform can be a significant breakthrough for complex electrofluidic arrays (increased size or resolution) with enhanced function, agility and programmability. An amorphous indium gallium zinc oxide (a-IGZO) semiconductor active layer is used because of its high mobility of 1–15 $cm^2\ V^{-1}\ s^{-1}$, low-temperature processing and transparency for potential spectroscopy and imaging. Several electrofluidic functionalities are demonstrated using a simple 2×5 electrode array connected to a 2×5 IGZO thin film transistor array with the semiconductor channel width of 50 μm and mobility of 6.3 $cm^2\ V^{-1}\ s^{-1}$. Additionally, using the TFT device characteristics, active matrix addressing schemes are discussed as the geometry of the electrode array can be tailored to act as a storage capacitor element. Finally, requisite material and device parameters are discussed in context with a VGA scale active matrix addressed electrofluidic platform.

Introduction

Significant effort has been devoted to develop highly integrated and automated lab-on-a-chip systems for miniaturized analysis in chemical and biological applications.[1,2] Lab-on-a-chip systems offer many potential advantages, including: (1) increasing both materials and time efficiency; (2) automating equipment/technician intensive functions; and (3) providing portability to bring testing into the field. To realize many of the potential advantages of lab-on-a-chip, microfluidics has been traditionally investigated using permanent geometries of continuous polymer or glass microchannels.[3] Continuous microchannels allow pressure driven flow control and electrokinetic transport, which are useful for a wide array of biomedical and analytical applications.[3,4] However, such lab-on-a-chip systems based on physical microchannels suffer from complex fabrication and complicated control for high level functionality, and are almost always application specific and far from a true 'laboratory'.[2,5] There have also been numerous demonstrations of programmable liquid transport, including surface energy defined virtual channels,[6] electrowetting droplet transport,[2,7–10] and dielectrophoresis.[11,12]

Electrically driven channel-free microfluidic devices can allow electronically reconfigurable 2-D movement on surfaces.[2,13,14] For parallel and simultaneous liquid operation on large scales, it is necessary that 2-D addressable electrode arrays are capable of electrically accessing each point independently in an $m \times n$ electrode array.[15] However, the electrode lines, which connect the inner electrodes in the $m \times n$ array to the external control circuit, can cause interference and limit the electrode array size if these lines are positioned in the electrode gaps. One option that has been demonstrated is multilayer arrangement of electrical connections, where each of its $m \times n$ electrodes is accessed directly and independently through a multi-level metallization.[15,16] Nevertheless, electrical addressability of lab-on-a-chip devices currently requires external switching devices for each individual electrode for droplet transport, merging, and splitting. Thus for complex arrays, many switching devices and interconnections are needed and scale directly with the number of elements (increased size or resolution). Therefore fabrication processes and cost can be complicated and expensive as the number of input–output connections becomes unwieldy. In order to reduce the number of control electrodes, a cross-referencing design has been demonstrated, where two parallel chips, each

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having line electrodes by a single-level metallization, were positioned orthogonally.[17] Using a time-multiplexed driving scheme of the row and column electrodes with opposite signals, the electrode intersections become most hydrophilic, and thus, the droplet moves toward them. However, functionality, such as splitting along the column direction, and driving voltage are limited due to its structure.

This problem can be overcome if an active matrix (AM) addressing method using thin-film transistors (TFTs) is integrated with electrowetting or dielectrophoresis control ($m + n$ interconnections for the $m \times n$ element array), as is used in liquid crystal display technologies.[18] Active matrix addressing is a convenient addressing scheme used in video displays in which gate pulses with a certain pulse width are scanned from the 1st to the last gate electrode sequentially. To address an (m, n) pixel, where m is the m^{th} gate row electrode and n is the n^{th} source column electrode, the n^{th} column source pulse is applied during the m^{th} row gate pulse. During the off-period of the gate pulse, the charge in the selected pixel is stored due to pixel capacitance until the next gate pulse is applied. Because all m^{th} row TFTs are turned on when a single m^{th} gate pulse is applied, multiple pixels can be addressed by concurrently selecting multiple column source electrodes. AM technology currently supports pixel sizes of <50 μm (>300 pixels per inch displays) which would be 20× smaller than the mm sized electrodes used for conventional electrowetting lab-on-a-chip, enabling more precise and smaller volume mixing/dosing/splitting. In addition, a high resolution active-matrix would allow variable electrode geometries that can be optimized for each function (splitting, merging, and transport), unlike the conventional approach that is typically limited to only square electrode shapes.[8] Furthermore, although active matrix addressing provides superior functionality and configurability, its manufacturing cost can actually be lower because high-volume manufacturing of standard active-matrix backplanes can be simply programmed by software to adapt to smaller or niche applications.

For AM addressing, TFTs are used as switching devices, where conventional active matrix flat panel displays typically employ hydrogenated amorphous or polycrystalline silicon as the semiconducting active layer. However, Si-based TFTs are not transparent to visible light and amorphous silicon TFTs have a low mobility of <1 $cm^2\ V^{-1}\ s^{-1}$,[19] thus making it challenging to implement optical imaging or spectroscopy, and to use high capacitance electrowetting control or high frequency dielectrophoresis control. Polycrystalline silicon TFTs have a high mobility of ~100 $cm^2\ V^{-1}\ s^{-1}$, but high temperature processes are needed, so the use of low-cost and large-area glass and polymer substrates is not allowed.

Recently, transparent amorphous oxide semiconductors have been intensely studied for thin-film transistor arrays for AM display applications because of their high mobility of 1–15 $cm^2\ V^{-1}\ s^{-1}$ allowing logic inverters and ring oscillators with operations at frequencies as high as 2.1 MHz and low-temperature processing from room temperature to 350 °C allowing the use of low-cost and large-area glass and polymer substrates.[19–23]

In this paper we demonstrate the addressability of electrofluidic devices with amorphous indium gallium zinc oxide (a-IGZO) thin film transistor arrays. This work represents a significant step toward a fully programmable active matrix lab-on-a-chip. Fig. 1a shows a prospective schematic diagram of an electrofluidic device integrated on the TFT array. The bottom electrodes of the electrofluidic device are simply connected to the TFT electrodes through a *via* hole. While a complete integration is being developed, as an intermediate demonstration and validation, a TFT array was connected to electrofluidic devices using the interconnection scheme discussed below. Several important electrofluidic functionalities are demonstrated using a 2 × 5 electrode array connected to a 2 × 5 IGZO thin film transistor array with an active semiconductor channel width of 50 μm and mobility of 6.3 $cm^2\ V^{-1}\ s^{-1}$. Additionally, using the TFT device characteristics, active matrix addressing schemes are discussed as the geometry of the electrode array can be tailored to act as the storage capacitor element. Finally, necessary parameters are discussed for optimal active matrix addressing from device measurements.

Experimental

TFT fabrication

A 5 × 5 TFT array using an inverted staggered structure was fabricated using an a-IGZO film as the semiconductor n-channel active layer. A chromium (Cr) gate metal (150 nm) was sputter deposited onto a 500 nm SiO_2 coated silicon wafer and subsequently lithographically patterned and wet chemically etched with a standard Cr wet etch solution (9% $(NH_4)_2Ce(NO_3)_6$ + 6% $(HClO_4)$ + H_2O). A SiO_2 gate dielectric (100 nm) layer was deposited via plasma enhanced chemical deposition (PECVD). The a-IGZO active layer (50 nm) was deposited by rf-magnetron sputtering using a 2 inch diameter target (In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 1 mol%) at room temperature. The rf sputtering power was 60 W and the sputtering pressure was 5 mTorr with a 20 : 5 mixing ratio of argon and oxygen, respectively, at a fixed total flow rate of 25 sccm. The a-IGZO active area was photolithographically patterned and etched using diluted 0.1% buffered oxide etchant. Au/Ti (80/10 nm) source and drain electrodes were deposited by e-beam evaporation and patterned by a lift-off method. The TFT semiconductor channel width (W) and length (L) were 50 and 20 μm, respectively. Finally, the samples were annealed at 350 °C in nitrogen ambient for 1 h. Fig. 1b and c show a photograph of a fabricated 5 × 5 IGZO TFT array and a cross-sectional view schematic, respectively. Fig. 1d shows the schematic diagram of an electrical driving system developed for active matrix addressing of the IGZO 5 × 5 TFT array. A pulse generating program was developed using LabView software. This program controlled the data acquisition (DAQ) card to send control signals to solid state relays (Vishay Semiconductors LH1512BB). During operation, 2 external power supplies (Keithley Model 2400 Sourcemeter) and 10 relays were used. Relays were inserted between power supplies and gate and source electrodes, as shown in Fig. 1d. During the testing the relays used 5 V signals generated by the DAQ card, and higher voltages were then applied to the IGZO TFT array platform. Electrical connections between the TFT array and the electrofluidic pixels were made using a customized test clip with spring load pins. For the active matrix testing and characterization, an unpassivated TFT array was used and the interconnection scheme is illustrated in Fig. 1f.

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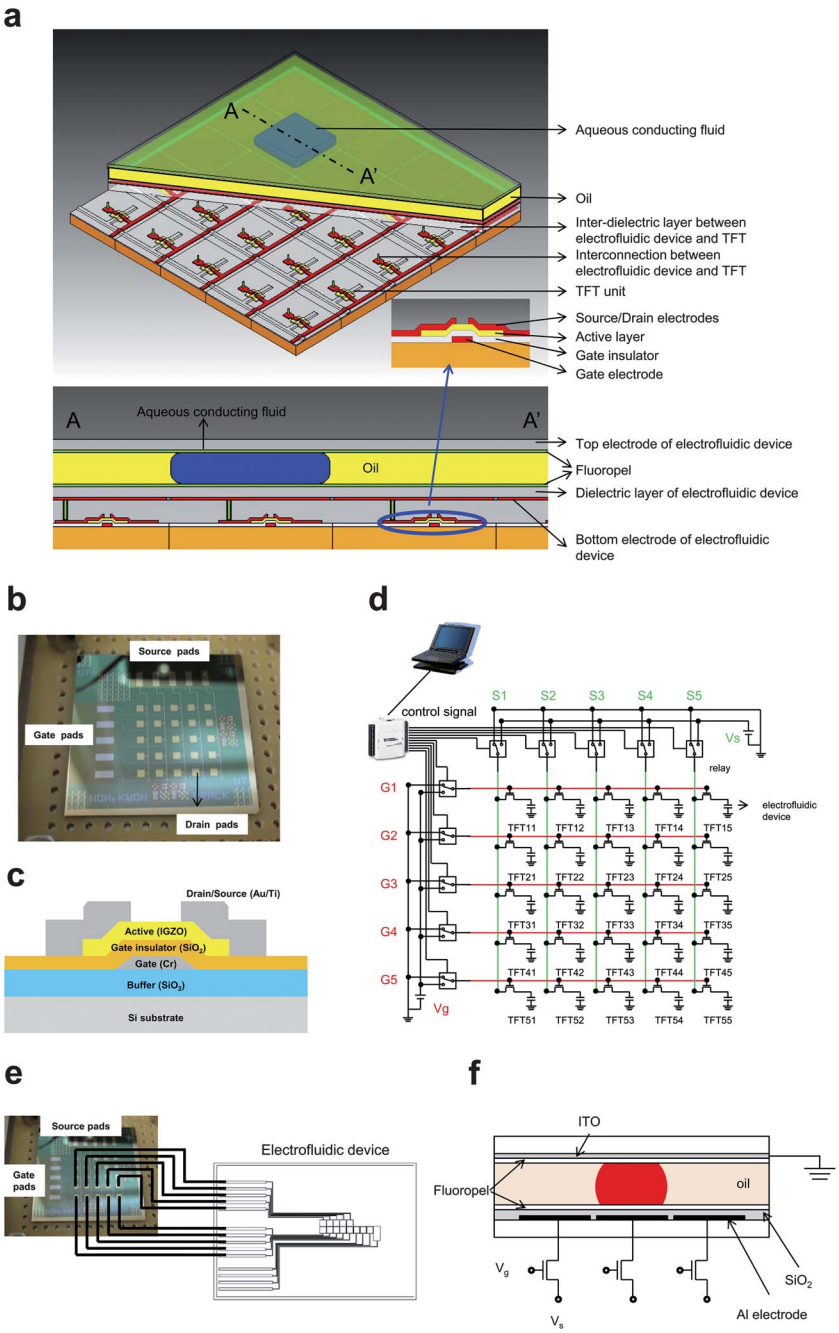


Fig. 1 (a) Prospective schematic diagram of an electrofluidic device integrated on the TFT array. (b) Photograph of a 5 × 5 IGZO TFT array. (c) Cross-sectional view of IGZO TFT. (d) Schematic diagram of a TFT array driving system. (e) Illustration of interconnection between TFT array and electrofluidic device. (f) Cross-sectional view of an electrofluidic device.

Electrofluidic device fabrication

Electrofluidic devices consisted of a 2 × 5 array of interdigitated electrodes with a pitch of 2.54 mm. The bottom glass plate was coated with a 100 nm thick Al layer by e-beam evaporation and patterned using the lift-off method. Subsequently, a 200 nm thick SiO_2 dielectric layer was deposited by plasma enhanced chemical deposition (PECVD). The electrofluidic top plate consisted of an indium-tin oxide (ITO) coated glass. The bottom and top plates were then dip-coated in Cytonix Fluoropel 1601 V solution with a 2.5 mm s^{-1} pulling speed and baked for 30 min at 140 °C to form a hydrophobic fluoropolymer film of ~50 nm thickness and a low surface energy of ~16 mN m^{-1}. Because the fluoropel was deliberately thin, the film was hydrophobic however not electrically insulating; thus the ITO electrode on the top plate was effectively electrically conductive with any fluid in the channel. A glass spacer was used to create the requisite gap of 160 μm between the top and bottom plates. Before clamping, an aqueous conducting fluid of ~1 μl was dosed on the Al electrode. For visualization, a 10 wt% red pigment with 0.01 wt% of sodium lauryl sulfate was dispersed in the fluid. The top and bottom plates were then clamped, and an insulating silicone oil (Dow

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Corning OS-30 oil) was infiltrated into the gap between the plates. The interfacial surface tension between the conducting pigment dispersion and insulating oil was $\gamma_{ci} \approx 50$ mN m^{-1}. The non-actuated contact angle of the liquid was 160–180°.[24] The fluoropel was so leaky that there was no measurable charge trapping or injection. Fig. 1f shows the cross-sectional schematic of the completed electrofluidic device.

Results and discussion

TFT electrical properties and TFT driven electrofluidic device

Transistors consist of three electrodes commonly called gate, source, and drain, as shown in the inset of Fig. 2a. When the TFT electrical properties are measured, one electrode (usually source electrode) is grounded. When a bias (V_{DS}) is applied to the drain electrode, drain current (I_{DS}) flows, which is modulated by gate voltage (V_{GS}). If V_{GS} is smaller than a threshold voltage (V_T), very small I_{DS} flows, but if V_{GS} is higher than V_T, the drain current (I_{DS}) is dramatically increased. Therefore, transistors can be used as an efficient switching device in electronics.

Fig. 2a shows the transfer characteristics (drain current I_{DS} as a function of the gate-to-source voltage V_{GS}) of 15 IGZO TFTs (rows 1–3). The drain-to-source voltage V_{DS} was kept at 30 V. The IGZO TFTs demonstrate good electrical performance and uniformity. The saturation field effect mobility μ_{FE} and threshold voltage V_T were calculated using the saturation current equation, $I_{DS} = (1/2)\ \mu_{FE}C_i(W/L)(V_{GS} - V_T)^2$, where C_i is the capacitance of the gate insulator. The TFTs operated in the normally off mode with μ_{FE} of 6.3 ± 0.18 cm^2 V^{-1} s^{-1} and V_T of 6.6 ± 0.49 V, respectively. The off-currents at $V_{GS} = 0$ V were ~10^{-9} A, corresponding to ~30 GΩ off-state resistance.

In order to use a TFT as a switching device for the electrofluidic device, the drain electrode of the TFT was connected to the electrode of the electrofluidic device. A voltage was applied to the source electrode, as shown in the inset of Fig. 2b and c. Because of the leakage current through the electrofluidic device, there was a slight voltage drop across the TFT; therefore the applied voltage at the source electrode was not exactly at the drain electrode. To determine the real driving voltage of the electrofluidic device with the TFT connected to it, the source voltage was applied to the source electrode of the TFT. Then the voltage at the drain electrode, which is the actual driving voltage of the electrofluidic device (V_E), was measured as a function of the gate voltage V_G and the source voltage V_S. (In order to avoid confusion, V_G and V_S notations were used when connected to the electrofluidic device as distinguished from V_{GS} and V_{DS} for standalone TFT operation.) Fig. 2b shows V_E as a function of V_G when V_S was maintained at 20 V for the 3 TFTs (TFT 11, TFT 21, and TFT 31). When V_G was 0 V, V_E was also ~0 V,

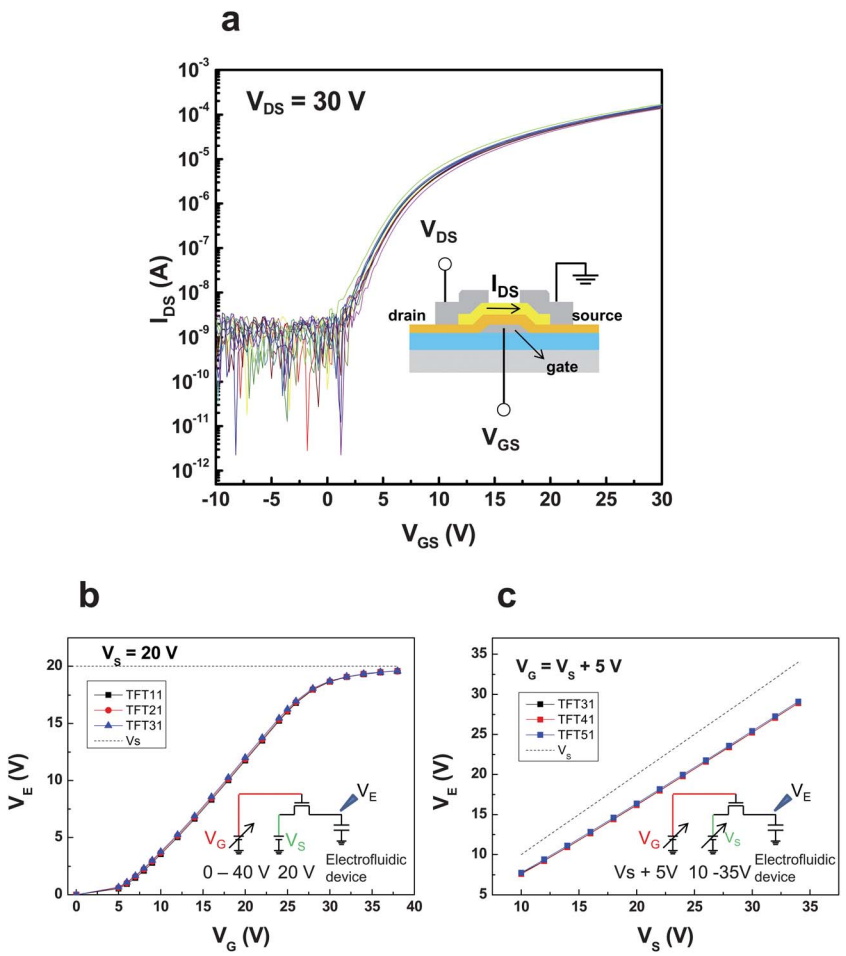


Fig. 2 (a) Individual TFT transfer characteristics. TFT output voltage V_E as a function of (b) V_G and (c) V_S.

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which means the entire V_S was dropped across TFT. As V_G was increased and the TFT channel resistance decreased, V_E increased and the voltage drop across the TFT ($V_S - V_E$) decreased. Fig. 2c shows V_E as a function of V_S. The power consumption can cause temperature elevation in the device. Practically, when the TFT was connected to the electrofluidic device serially, and $V_S = 35$ V and $V_G = V_S + 5$ V $= 40$ V, the voltage drop across TFT was about 5 V and the total current was less than 1 μA. The power consumption across TFT was less than 1 μW (5 V × 1 μA), therefore the temperature elevation in the device is negligible.

To assess the capability of the TFTs to drive electrowetting without compromise in droplet transport speed, droplet transport velocities were compared for both solid state relay and TFT driven electrofluidic devices. In the case of the relay driven electrofluidic devices, each electrode was connected directly to the relay. As the relay has very low on-state resistance (10 Ω), the voltage drop across the relay is virtually 0 V. In the case of the TFT driven electrofluidic device, each electrode of the electrofluidic device was connected to a drain electrode of a TFT. Constant source voltage was applied on the source electrodes of all TFTs and the gate voltage of each TFT was modulated to drive electrowetting. The droplet transport velocity was calculated from the moving time of the droplet leading edge across the electrode pitch of 2.54 mm by image analysis. According to the electrode position, there were deviations of droplet transport velocity because droplet transport is sensitive to the surface condition and gap height. As shown in Fig. 3a, the droplet transport velocity for the TFT driven electrofluidic device was slightly slower than for the relay driven electrofluidic device at the same applied voltage because of the slight voltage drop across the TFT, in agreement with the data of Fig. 2. When the supplied voltage is replaced with the real driving voltage (V_E) for the TFT (Fig. 2c), as expected, there is no difference in the droplet transport velocity between the relay and TFT driven electrofluidic device. Fig. 3b shows the velocity$^{1/2}$ *vs.* voltage plot (where V_E was used for the TFT driven electrofluidic device using the relationship of V_S and V_E from Fig. 2c). The linear relationship between the square root of droplet velocity and voltage was obtained which is consistent with what has been reported previously.[25] The linear fit line is shown as the blue dashed line.

Active matrix driven electrofluidic devices

Beyond the TFT actuated electrofluidic transport, active matrix (AM) electrofluidic control was also explored. To show unique AM driven electrofluidic, two individual droplets were simultaneously controlled using a 2 (gate rows) × 5 (source columns) electrofluidic electrode array (Fig. 4). Gate pulses with 50 ms pulses width and 40 V amplitudes were sequentially applied to the two gate rows. Initially, two droplets were positioned at (G1, S4) and (G2, S2) with a combination of gate and source pulses, indicated as (1) in Fig. 4. Source pulses had 50 ms pulse widths and 35 V amplitudes. To simultaneously move the droplets upward and downward, the source pulses were changed, indicated as (2). Interestingly, droplets could not entirely move to the next electrodes during one 50 ms pulse sequence because the droplet transport speed was ~6 mm s^{-1} at a source voltage = 35 V. Therefore, these pulse combinations had to be maintained for a certain time (denoted as t_{moving}) to completely move the droplet from pixel to pixel, indicated as (3). For the current system, t_{moving} was ~3 s (or ~30 pulses). Future work will explore the effects of optimized electrode size, gap height, electrode dielectric, and droplet solution to enhance the droplet transport speed to established values of ~10 cm s^{-1}. Using various combinations of gate and source pulses further droplet motions were demonstrated, indicated as (4)–(8). A supplemental video is available in the ESI (Video S1†). As demonstrated in Fig. 4, the simultaneous and individual droplet control for 10 (2 × 5) electrodes was achieved using only 7 bias lines (2 gate and 5 source bias lines), which is the obvious merit of the AM driving method. If the electrofluidic device is scaled up with $m \times n$ elements for complex electrofluidic arrays, only $m + n$ bias lines are needed.

Additional functionalities obtained using AM driven electrofluidic devices that are important for lab-on-a-chip microfluidic applications. Continuous channel formation is demonstrated in the ESI (Video S2†). The continuous channel could be formed evenly across individual rows. Two dimensional "L" and "T" shaped channels are also demonstrated. However, this two dimensional channel cannot be maintained if the voltage is turned off. "L" or "T" shapes change to circular shapes due to surface tension. However, if the top plate is replaced by post-arrays or a so-called "Laplace barrier" structure,[26] off-state

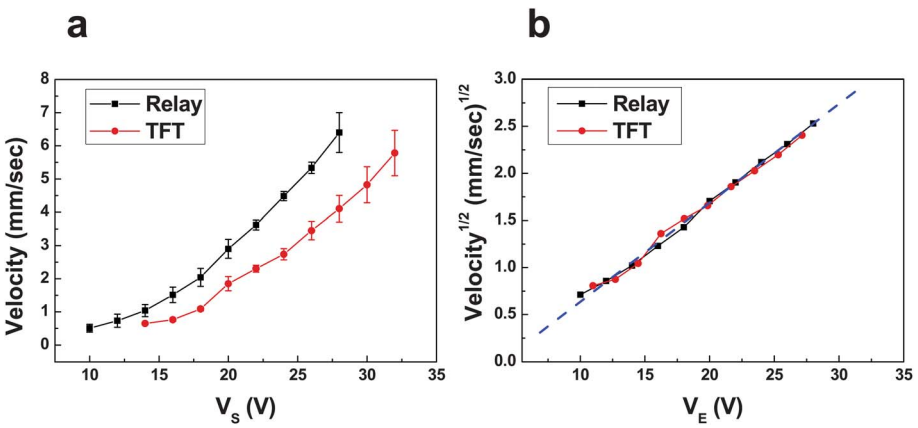


Fig. 3 (a) Electrowetting transfer velocity as a function of V_S. (b) Square root of the electrowetting transfer velocity plot as a function of V_E.

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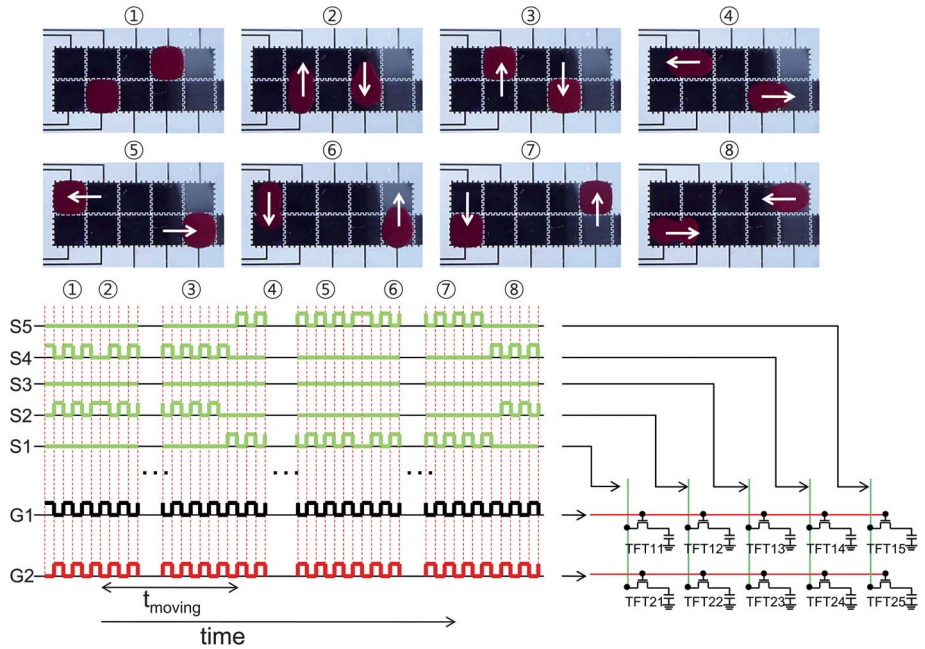


Fig. 4 Simultaneous and individual control of two droplets by an active matrix addressing method using an IGZO TFT array. Video S1 is available in the ESI†.

stability is possible and the channel shape can be maintained even when the voltage is turned off. Additionally, channel merging and splitting are demonstrated in the ESI (Video S2†).

Electrical analysis of active matrix driven electrofluidic device

Several additional observations for AM driven electrowetting droplet movement are worth noting. Interestingly, droplet vibration was observed during AM driving, as shown in ESI Videos S1 and S2†. In order to understand this vibration, we measured waveforms during gate and source pulsing using an oscilloscope, as illustrated in Fig. 5a. Fig. 5b shows the waveforms of the gate, source and electrowetting voltage. The gate pulse frequency was 5 Hz, the duty cycle was 50% and the source pulse width was set equal to the gate pulse width. The gate and source pulse amplitudes were 35 and 30 V, respectively. When the gate and source pulses were applied, ~5 V was dropped across the TFT and a V_E of ~25 V was induced at the electrofluidic device.

For the AM driving, V_E should be maintained during the subsequent gate pulse off period. However, the measured V_E showed a rapid decrease, reducing the electrowetting effect, which causes the droplet vibration during pulsing. At the end of the gate pulse off period (indicated with arrows in Fig. 5), V_E was 0 V. The voltage decrease is related to *RC* charging–discharging in the series circuit of the resistance and capacitance of the apparently leaky SiO_2 dielectric layer. The voltage discharging is expressed as $V_E = V_{E\,max} \times \exp(-t/\tau)$, where V_E is the voltage across the electrofluidic device, $V_{E\,max}$ is the initial voltage, t is the elapsed time, and τ is the *RC* time constant of the circuit. The leakage current through one electrode of the electrofluidic electrodes with a liquid droplet was individually measured and was determined to be in the range of 10–100 MΩ (denoted as R_E). The capacitance of one electrofluidic electrode (denoted as C_E) was calculated to be ~750 pF based on the dielectric constant and thickness of SiO_2 (3.9, 200 nm) and fluoropel (2.0, 50 nm) layers and the area of the electrode (0.0645 cm^2). Using the *RC* time constant of 7.5 ms (10 MΩ × 750 pF), the calculated voltage across the electrofluidic device is 1.74 V after 20 ms, which is in good agreement with the measured value of ~2.5 V. In order to slow down the discharging time, external storage capacitors were additionally connected to the electrofluidic device. Fig. 5c and d show the waveforms with the 10 and 100 nF external storage capacitors, respectively. At the end of the gate pulse off period, V_E was 11.8 and 20.2 V, corresponding to 47.4 and 84.2% of $V_{E\,max}$, respectively.

Two ways to keep V_E high during the gate pulse off period is to increase the electrofluidic device capacitance or the driving frequency. Fig. 5e shows the waveform with 10 nF external storage capacitor for the gate pulse frequency of 10 Hz and duty ratio of 50%, respectively, and the source pulse width was again set equal to the gate pulse width (50 ms). At the end of the gate pulse off period, V_E was 15.7 V, which is higher relative to the 11.8 V of the 5 Hz pulse frequency. With the current geometry and 10 nF external storage capacitor, using a typical drive frequency of 120 Hz (4 ms pulse width and 50% duty cycle) the voltage decreased only to 87.8% of $V_{E\,max}$, as shown in Fig. 5f. 60–120 Hz is a key frequency target as it is the commonly utilized frame rate for the hardware and software that controls pixels in AM liquid crystal displays. In the ESI†, supplemental videos are available that compare the droplet vibration as a function of frequency (ESI, Video S3†) and external storage capacitance. Additionally, droplet movement with and without an external storage capacitor (ESI, Video S4†) is demonstrated in which smooth droplet motion was observed as expected when the *RC* discharging time was sufficiently long. Practically, 1 or 2 capacitors are commonly used in AM-LCD, so the inclusion of a separate capacitor is not a critical problem in an AM driven

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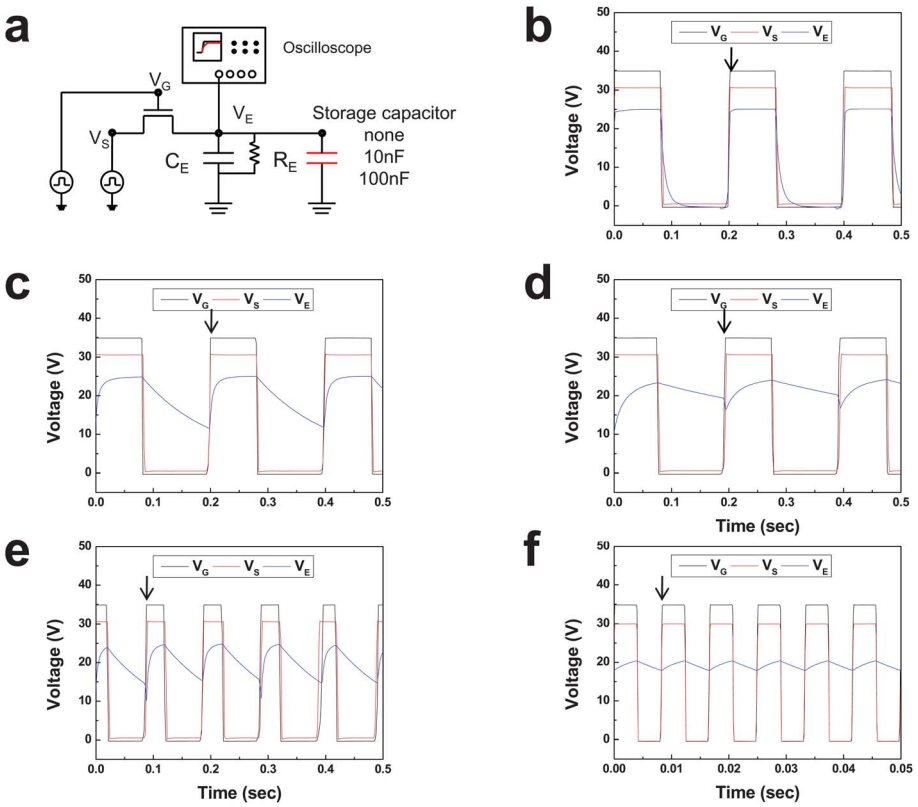


Fig. 5 (a) Schematic diagrams of waveform measurement. Gate, source, and electrowetting voltage waveforms as a function of an external storage capacitor with a gate pulse width of 100 ms, (b) only electrofluidic device, (c) electrofluidic device + 10 nF external storage capacitor, and (d) electrofluidic device + 100 nF external storage capacitor. Voltage waveforms for the electrofluidic device + 10 nF external storage capacitor with a gate pulse frequency of (e) 10 Hz and (f) 120 Hz (50% duty ratio).

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electrofluidic device. However, the capacitor pattern size should be considered when implemented in the TFT platform. For example, to achieve 10 nF capacitance using 100 nm thick SiO_2 (dielectric constant: 3.9), a square pattern with 0.54 cm length (area: $\approx$ 0.30 cm^2) is needed. This pattern size is too large to be implemented as a pattern in the TFT layer.

The most obvious way to decrease the discharging time and obtain a high *RC* time constant is to increase the resistance of the dielectric. The *RC* time constant can be expressed as $RC = \rho(t/A) \times \varepsilon_0\varepsilon_r(A/t) = \rho\varepsilon_0\varepsilon_r$, where ρ is the resistivity, ε_0 is the vacuum permittivity, ε_r is the relative dielectric constant, A is the area, and t is the thickness. Because resistivity and relative dielectric constant are intrinsic material parameters, the *RC* time constant is fixed regardless of pattern size when a single layer dielectric material is chosen. Thus, instead of single layer dielectrics, multilayer dielectrics, which consist for instance of polymer layers with low leakage current[27] and inorganic layers with higher dielectric constant, can be used to optimize the resistance and capacitance for optimal AM driving without significant loss of total capacitance.[20] Additionally, an improved aqueous solution (large ions) can be used to decrease dielectric failure in electrowetting systems.[28] In future work, an improved dielectric will be implemented to increase the resistance of the electrowetting dielectric.

Conversely, charging of the capacitor also slows as capacitance was increased and the gate pulse width was decreased. The charging time is expressed as $t_{charging} = C_{tot} \times V_E/I_{on}$, where C_{tot} is the total capacitance, and I_{on} is the on-state current of the TFT. Thus charging time can be reduced if the TFT mobility or current is increased. Since mobility is a materials constraint, a new design of TFT would be necessary to increase mobility. However, one can increase the TFT current by increasing the gate voltage and/or increasing the TFT semiconductor active channel width in the current TFT geometry.

From the above consideration of the electrofluidic/TFT properties, the necessary dielectric properties can be extracted for a scaled-up electrofluidic device with any number of gate rows, m. When the gate pulse width is chosen, t_G, the time of the gate off period is expressed as $t_G \times (m - 1)$. If a 10% voltage drop is tolerable to maintain an on-state and ensure smooth droplet movement, the gate off period time should be shorter than $\sim$0.105 times the *RC* time constant ($t_G(m - 1) < 0.105\tau$). Consequently, the dielectric material should be tailored to satisfy the necessary *RC* time constant. If the dielectric material itself cannot satisfy the necessary *RC* time constant, an additional storage capacitor can be implemented in the TFT array platform as is commonly used for AM LCD displays.

Additionally, the TFTs must be optimized for both ON and OFF state resistances to satisfy an active matrix drive scheme. Firstly, the ON state resistance of the TFT must be small enough, which can be achieved by increasing the gate voltage and/or by increasing the TFT semiconductor active channel width as

mentioned above, such that the TFT can fully charge the electrofluidic voltage (capacitor) during the gate row write time. This suggests that the $R_{(TFT\text{-}ON)}C_E$ time constant should be less than ~20% of the designed write time. Secondly, once a voltage is written to the electrofluidic device capacitor, the voltage has to be maintained during the entire frame (until the next voltage is written in the next frame). This requires that the time constant for the OFF state TFT resistance and electrofluidic device capacitance ($R_{(TFT\text{-}OFF)}C_E$) be much longer than the frame write time. This further requires that the R_E be similarly large such that it also satisfies an R_EC_E time constant much than the duration of each frame. To achieve for instance a typical VGA (640 columns × 480 rows) and assuming R_E is 1 GΩ, and C_E is 750 pF, and a 120 Hz frame rate (frame time = 8.3 ms, write time = 17.4 μs); the requisite ON and OFF state resistances for the TFTs are ~4.6 kΩ and ~1 GΩ respectively. This combination should be achievable by using multi-layer electrofluidic dielectrics (R_E > 1 GΩ) and increasing either (or a combination thereof) the gate voltage, the TFT mobility, and/or the channel width.

Conclusions

In conclusion, we have demonstrated herein a programmable electrofluidic platform driven by an active matrix addressing method using amorphous oxide thin film transistors. Because the active matrix addressing method minimizes the number of control lines necessary ($m + n$ lines for the $m \times n$ element array) and current amorphous oxide thin film transistors support active matrix technology with pixel sizes of <50 μm (>300 pixels per inch displays), the active matrix addressing method integrated with the electrofluidic platform can be a significant breakthrough for complex electrofluidic arrays (increased size or high resolution) with enhanced function, agility and programmability. Future work will focus on the full integration of the electrofluidic platform on a fully transparent TFT platform. Furthermore, we will explore different hybrid dielectrics for optimum large-scale platforms as well as investigate different dimensionality to mimic a synthetic "vascular system" in which both high throughput and small volumes can be controlled for true lab- and systems-on-chip. Fully transparent TFT backplanes and the high electrical performance that amorphous oxide semiconductors provide will allow optical analysis or sensing for life and chemical sciences on a complex programmable electrowetting platform, therefore promise significant functionality.

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